Performance Analysis of 10 nm FinFET with Scaled Fin-Dimension and Oxide Thickness

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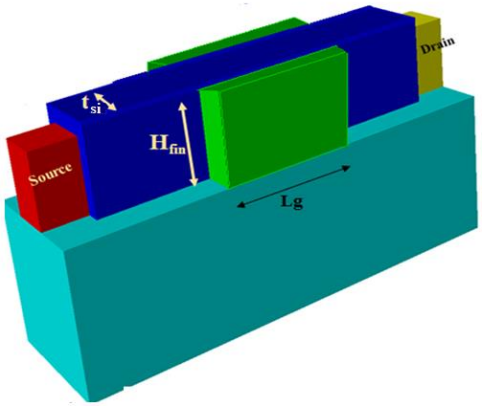
***Abstract* — This research work presents the performance analysis of multi-gate FinFET structure simulated at *10-nm* technology node. The device electrical parameters have been extracted at different Fin dimensions to analyze the effect of Fin-scaling and oxide thickness variation onto the device performances. The designed device has been simulated at different heights and widths of the Fin. Thereafter, the oxide thickness has been varied for the structure. The effects of Fin height, width, and oxide thickness variation have been reported. The minimum value of Drain Induced Barrier Lowering (DIBL) has been observed at H_{fin} *of* 27 *nm* with I_{ON}/I_{OFF} ratio as 1.89×10^4 to 3.1×10^4. The lowest Subthreshold Swing (SS) of *59.5 mV/decade* is obtained at H_{fin} *of 40 nm.* At different Fin-width values, it has been observed that the DIBL reduces with the reduction in Fin-width but the drain current increases only with higher Fin-width and hence, ON current increases. This research work provides a better understanding to the scaling of the complex structure design of FinFETs.**

Keywords* — *DIBL, Short channel effects, Scaling, SOI-FinFET, Process parameter variation, Microelectronics, VLSI.

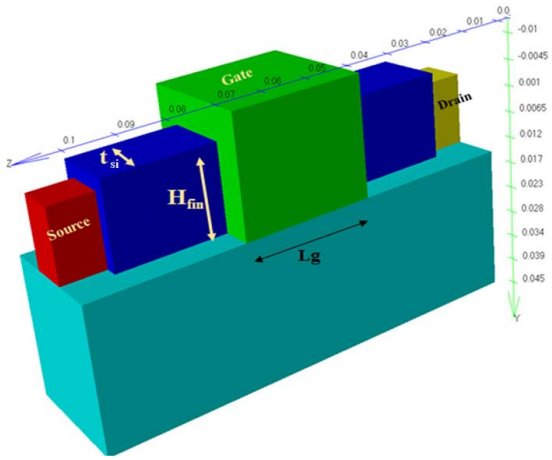
I. INTRODUCTION

As the transistors dimensions are shrunk below *100 nm* researches are very actively pointed to nanometers regime and make it possible to package millions of transistors in a single chip with VLSI and ULSI technology. The miniaturization of electronic devices has led the semiconductor industry step forward to its technological progression. The integrated circuits which follow Moore's law have become so smaller that the scaling of the conventional MOSFET has become ever more difficult because it is facing atomic and quantum-mechanical boundaries [1, 2]. It has become difficult to minimize (zero) the channel current due to Short Channel Effects (SCEs). To overcome these, several efforts have been made and different architectures i.e. more than one gate structures and thin channel devices have been modeled and proposed as future prospective [3-5]. The FinFETs are amongst one of the capable semiconductor devices which are switched to scale further cutting-edge processes in industry. Performance analysis of FinFET to MOSFETs have been done at *14-nm* technology node [6, 7]. Recently, the technology node of FinFET has reduced to *10-nm* technology [8, 9].

Structural dimensions are very important to determine the transistor size. The 3-D analysis with inclusion of the size parameter is required to identify the best performance of simulated device. In this work, authors have designed and simulated a multi-gate FinFET structure at gate length *20 nm* and extracted its parameters at different Fin-dimensions. The impact of Fin-width, height, and oxide thickness variation on the electrical characteristics such as Drain Induced Barrier Lowering (DIBL), Subthreshold Swing (SS), transconductance, and transfer characteristics have been cahracterized. This paper is organized as follows. Section II describes the proposed novel device structure. In Section III, simulated response and various analysis have been specified to understand the mechanism. Finally, the Section IV concludes the work and recommends the future aspects.



(a)



(b)

Fig. 1. Schematic representation of proposed device structure (a) Independent Gate (IG) FinFET (b) short gate (SG) FinFET.

II. Proposed Device Structure

Fig. 1 shows the schematic of the proposed FinFET structure Independent-Gate (IG) FinFET and Short-Gated (SG) FinFET. In this structure dimensions H_{fin}, T_{si}, t_{ox}, and L_g refers to the silicon Fin-height, Fin-width, gate-oxide thickness, and the gate length of the device, respectively. The stucture is made on insulator substrate, because the Silicon-on-Insulator (SOI) devices are much flexible in comparison to the bulk-Si substrate [10, 11].

The device structural parameters include gate length (L_g) *20 nm*, oxide thickness (t_{ox}) *2.5 nm*, fin height (H_{fin}) *27 nm - 40 nm*, fin width (T_{Si}) *4 nm - 8 nm*, and the fin pitch *30 nm* based on ITRS *10-nm* technology node [12]. The FinFET structures have supply voltage (V_{dd}) *0.8 V*, gate work function is *4.49 eV* for low-power application and source-drain-channel doping concentration in the range of $1\times e^{+16}/cm^3$ to $1\times e^{+19}/cm^3$.

The gate electrode is positioned on top of an insulator which covers the channel region. The channel electro-statistically controlled by the gate using capacitive coupling of gate and the channel region, through insulator. The scaling laws require a reduction in the depth of the source and drain regions by the same scaling factor as the gate-length reduction.

III. Analysis of Various Parameters

Device structure variation in FinFET dimension and the extracted parameters have been explained in this section. As shown in Table I, authors simulated the device model for the Fin height to gate length ratios, H_{fin}/L_g of *1.35*, *1.5* and *1.8*. Then the device simulation results at varying Fin-width to gate length ratios, T_{si}/L_g of *0.4*, *0.3* and *0.2*. Further, the oxide thickness has been varied to *0.5 nm*, *2 nm and 5 nm* each time in the structure to observe the the impact on device characteristics.

A. *Effect on parameters at Fin height (H_{fin}) variation*

Fig. 2 shows the transfer characteristics at gate length *20 nm* with different H_{fin}/L_g (1.35, 1.5, 1.8, and 2.0). Simulation results shows that drain current increases with the increase in the height of the Fin. The extracted electrical parameters from the obtained simulated results at different Fin heights are listed Table II. It can be observed that I_{ON}/I_{OFF} and DIBL increases with the increase in height, whereas threshold voltage and SS decreases.

It can be clearly observed from Fig. 2 that the increase in Fin height makes the channel larger to accumulate more charges in the region and increases current densities near the drain electrodes to compose the higher drain current.

TABLE I. FinFET Device Parameters

L_g *(nm)*	20	20	20	20
H_{fin}/L_g	1.35, 1.5, 1.8	1.35	1.35	1.35
T_{si}/L_g	0.4	0.4, 0.3, 0.2	0.5	0.4
L_{ol}/L_g	0.2	0.2	0.1, 0.2, 0.5	0.2
t_{ox} *(nm)*	2.5	2.5	2.5	0.5, 2, 5

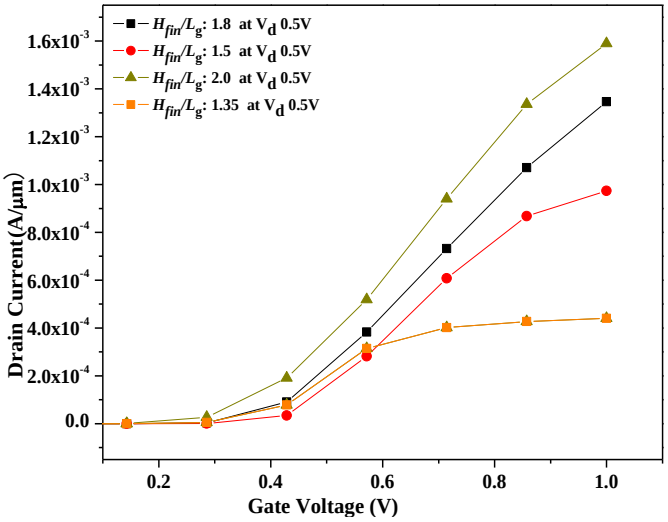


Fig. 2. Transfer characteristics of the device with a gate length L_g=20nm and H_{fin}/L_g = 1.35, 1.5, 1.8 and 2.0 at V_d = *0.5V*.

TABLE II. Extracted Parameters at Different Fin Height (H_{fin})

H_{fin}/L_g	L_g *(nm)*	V_T	*SS*	I_{ON}/I_{OFF} *(Vd 0.05V)*	I_{ON}/I_{OFF} *(Vd 0.6V)*	*DIBL mV/V*
1.35	20	0.438	77.348	1.89×10^4	3.1×10^4	23.99
1.5	20	0.530	67.326	2.88×10^4	2.9×10^5	37.11
1.8	20	0.551	63.395	5.53×10^5	3.0×10^5	43.68
2	20	0.597	59.535	4.92×10^5	4.1×10^6	66.79

B. *Effect on parameters at Fin-width (T_{si}) variation*

The transfer characteristics of the device at gate length *20 nm*, with different T_{si}/L_g (*0.5, 0.4, 0.3, 0.2*) at V_d *0.5V* and *1 V* are shown in Fig. 3 and Fig. 4, respectively. Drain current with respect to the Fin-width and gate voltage varying from *0 V* to *1 V* shows in the figures that as the thickness of the fin increases both the on current and off current increases.

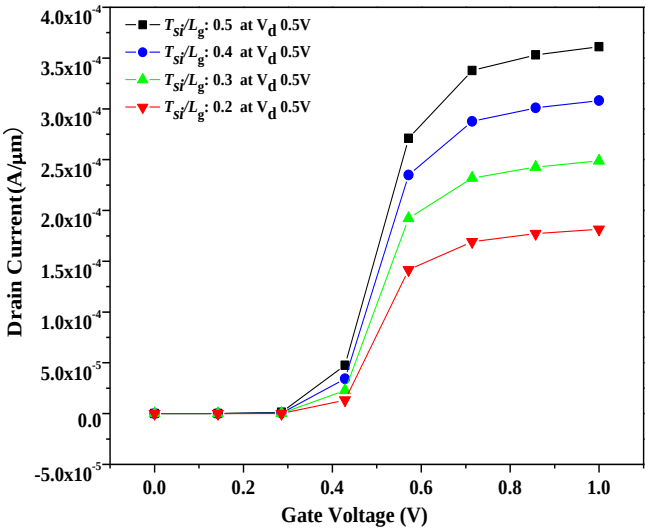


Fig. 3. Transfer characteristics of the device with a gate length L_g=20nm and T_{si}/L_g = 0.5, 0.4, 0.3 and 0.2 at V_d = *0.5V*.

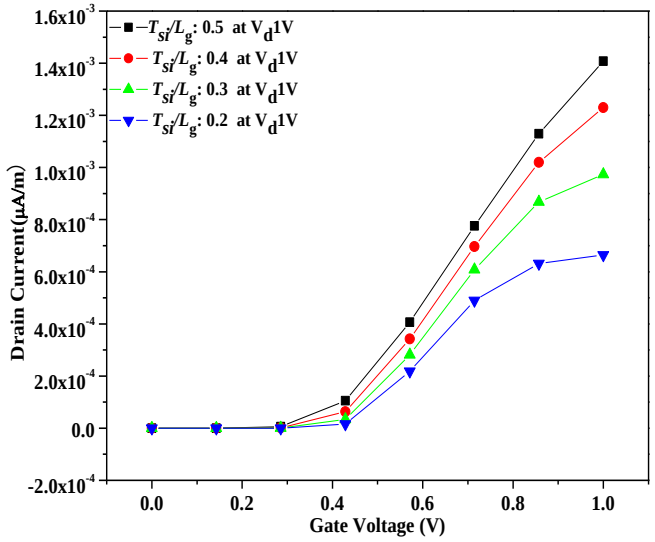


Fig. 4. Transfer characteristics of the device with a gate length L_g=20nm and T_{si}/L_g = 0.5, 0.4, 0.3 and 0.2 at V_d =*1V*.

TABLE III. EXTRACTED PARAMETERS AT DIFFERENT FIN-WIDTH (T_{si})

T_{Si}/L_g	L_g in (nm)	V_T	SS (mV/decade	I_{ON}/I_{OFF} Vd 0.05V	I_{ON}/I_{OFF} Vd 0.6V	DIBL mV/V
0.5	20	0.490	73.05	9.76×10^{5}	3.1×10^{6}	66.98
0.4	20	0.508	67.24	8.38×10^{4}	2.9×10^{5}	42.50
0.3	20	0.528	65.72	3.27×10^{3}	3.0×10^{3}	27.36
0.2	20	0.550	62.29	5.64×10^{2}	4.1×10^{2}	23.07

The electrical parameters calculated from the results of simulation of the proposed device at Fin-width *0.5, 0.4, 0.3* and 0.2 are listed in Table III. Higher on current is obtained at larger T_{Si}/L_g, Fin thickness ratio with respect to the gate length at lower threshold voltage of 0.49 V. However, the DIBL increases 65.55% with 6 *nm* increase of Fin-width.

C. Effect on parameters at lap distance(L_{ol}) variation

The effect of varying the lap distance with gate and channel has been investigated using variation in gate-lap distance to the gate length ratio, L_{ol}/L_g of 0.1, 0.2 and 0.5 in each case. The obtained parameters when the gate lap distance is changed are listed in Table IV. The behavior of transconductance (G_m) at T_{si}/L_g *(0.5, 0.4, 0.3 and 0.2)* of the device with the gate voltage is presented in the form of graphs.

The transconductace is at the peak near the V_T of the perticular design of the device and it reduces with the lower T_{si}/L_g as depicted in Fig. 5. The maximum value of transconductance obatined at drain volatge *0.5 V* is 1.57×10^{-3} *S/μm* at T_{si} is *10 nm*. Fig. 6 shows the highest value of transconductance at drain volatge *1 V* is 2.49×10^{-3} *S/μm* at T_{si} is *10 nm*. The transconductance decreases with the decrease in Fin-width.

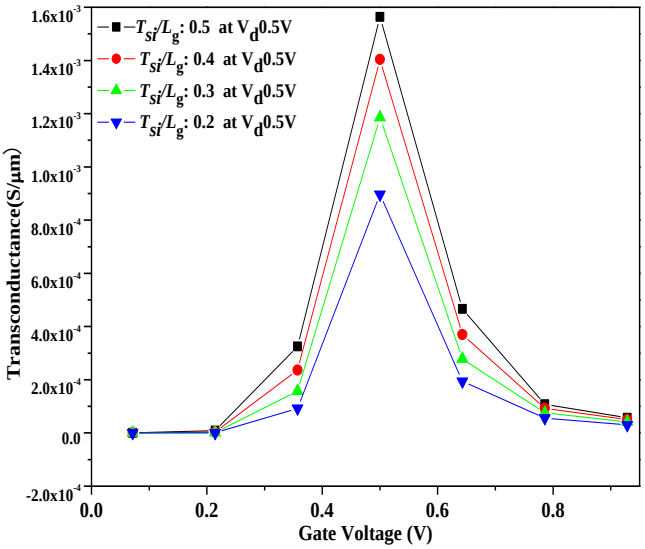


Fig. 5. Transconductance versus gate voltage with T_{si}/L_g = 0.5, 0.4, 0.3 and 0.2 at V_d = *0.5V*.

TABLE IV. EXTRACTED PARAMETERS AT DIFFERENT GATE LAP DISTANCE

L_{ol}/L_g	L_g in (nm)	V_T	SS (mV/decade)	DIBL mV/V
0.1	20	0.497	71.69	61.03
0.2	20	0.527	65.72	27.35
0.5	20	0.502	56.20	76.49

The extracted electrical parameters when the gate overlap distance is varied are listed in Table IV. The minimum of threshold voltage is 0.497 V obtained at gate overlap distance is 2 *nm* each side towards the source and drain. Significant subthreshold is observed when L_{ol}/L_g is 0.5, as to the gate overlap increases trapped charge density in the gate-oxide interface.

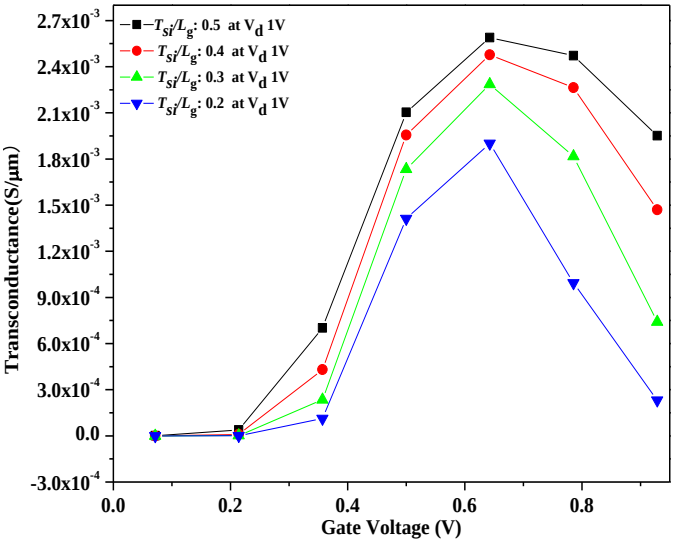


Fig. 6. Transconductance versus gate voltage with Tsi/L_g = 0.5, 0.4, 0.3 and 0.2 at V_d = *1V*.

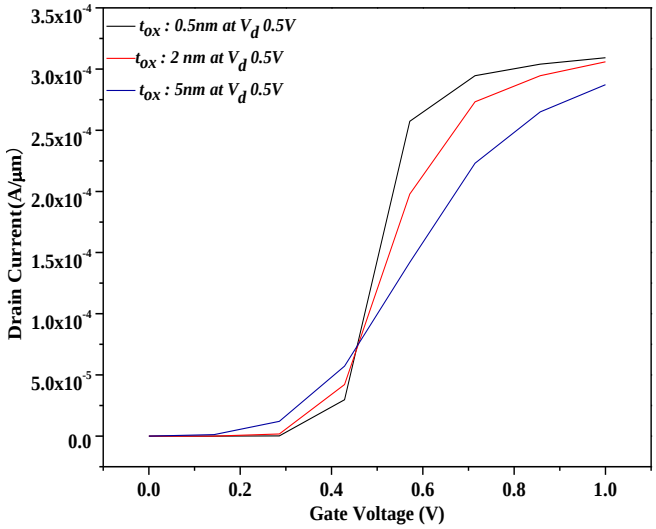


Fig. 7. Transfer characteristics with a gate length L_g=20nm and T_{si}/L_g=0.4 and t_{ox}= *0.5nm, 2nm* and *5nm*.

TABLE V. EXTRACTED PARAMETERS AT DIFFERENT GATE OXIDE THICKNESS (t_{ox})

$t_{ox\ (nm)}$	L_g *in (nm)*	V_T	*SS (mV/decade)*	*DIBL mV/V*
0.5	20	0.508	65.36	27.051
2	20	0.508	78.63	89.114
5	20	0.516	110.63	262.669

The extracted electrical parameters when the gate overlap distance is varied are listed in Table IV. The minimum of threshold voltage is 0.497 V obtained at gate overlap distance is 2 *nm* each side towards the source and drain. Significant subthreshold swing is observed when L_{ol}/L_g is 0.5, as to the gate overlap increases trapped charge density in the gate-oxide interface.

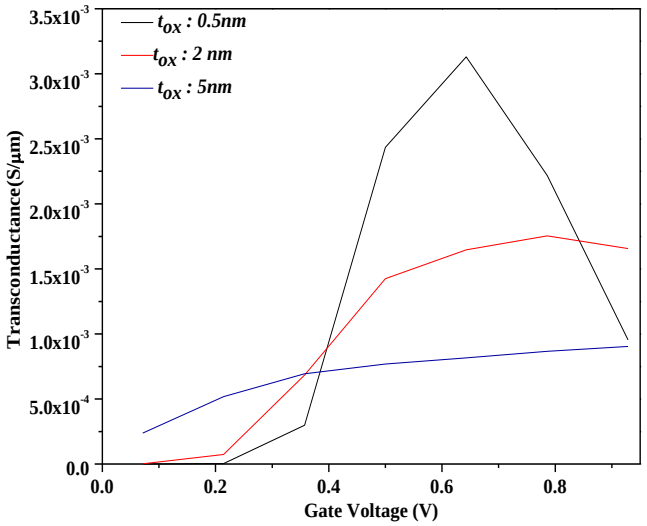


Fig. 8. Transconductance versus gate voltage at various t_{ox} *(0.5 nm, 2 nm and 5 nm).*

D. Effect on parameters at oxide thickness (tox) variation

The gate-oxide thickness in the structure is varied from *0.5 nm* to *5 nm.* The tranfer characteristics as a result obtained at different oxide thicknesses are shown in Fig. 7. Transconductance, G_m at various t_{ox} *(0.5 nm, 2 nm and 5 nm)* is extracted for range of the gate voltages and is displayed in Fig. 8. It can be seen that when the oxide thickness is approaching closer to the Fin-width the there is no significant device current is available and the transconductance obtained is very low. Table V list extracted parameters at the different oxide thickness in the simulation of the device.

The extracted electrical parameters when the gate overlap distance is varied are listed in Table IV. The minimum of threshold voltage is *0.497 V*.

IV. CONCLUSIONS AND FUTURE ASPECTS

In this work, a multi gate FinFET structure has been designed and simulated at 10nm-technology node. The device electrical parameters have been extracted at different Fin dimensions. We have analyzed the electrical behavior of the device by means of transfer characteristics, transconductance, and the extracted parameters i.e. drain induced barrier lowering, subthreshold swing and device currents to report the impact of Fin dimension and oxide thickness variation on to the device performance. The device is simulated at Fin height to gate length ratios, H_{fin}/L_g of *1.35, 1.5* and *1.8* and Fin-width to gate length ratios T_{si}/L_g of *0.4, 0.3* and *0.2*. Further, the oxide thickness has been varied as *0.5nm, 2nm and 5nm* in the structure.

As results of Fin height variation it is reported that the drain current increases with the increase in the height of the Fin. The device current on to off ratio I_{ON}/I_{OFF} and DIBL increases with the increase in height while threshold voltage and SS decreases.The minimum value of DIBL is observed at H_{fin} *of* 27 *nm* with I_{ON}/I_{OFF} ratio as $1.89 \times 10^4 \sim 3.1 \times 10^4$. The lowest subthreshold swing, SS *~59.5 mV/decade* obtained at H_{fin} *of* 40 *nm.*

At different Fin-width the drain current variation with respect to the fin width and gate voltage varying from 0V to1V, it is observed that the DIBL reduces as the reduction in Fin-width but the drain current increases only with higher Fin-width and so as the on current and off current increases. The transconductance, G_m reduces with the lower T_{si}/L_g. The value of G_m obtained in the range of 1.57×10^{-3} *S/μm* ~ 2.49×10^{-3} *S/μm* with drain voltage ~ 0.05-1V at Fin-width of *10 nm*. The increase in the oxide thickness to the near T_{si} reduces device current drastically and the transconductance is very low. These outcomes of the work can be used for improved scaling of the semiconductor design of more complicated multi-gate device structures.

Device optimization solely depends on the width of the transitor, hence Fin-width scaling may lead to provide improved performance of the device. Further, circuit level simulation of the FinFETs with scaled Fin-dimension can be done for the assessment of the device performance as the furture scope of the work.

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